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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,215	09/09/2003	Francois Roy	S1022.81038US00	2710
23628	7590	02/03/2005	EXAMINER	
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			VU, QUANG D	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/658,215

Applicant(s)

ROY, FRANCOIS

Examiner

Quang D. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8-12 and 16 is/are rejected.
- 7) ☒ Claim(s) 5-7 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claim 14 is objected to because of the following informalities: The second claim 14 must be changed to claim 16. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 8-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of US Patent No. 5,163,179 to Pellegrini and US Patent No. 6,563,101 to Tullis.

Regarding claim 1, AAPA (figures 1-4) teaches a monolithic photodetector comprising:

a first active area (10) of doped single-crystal silicon corresponding to first (D2) and second (D3) photodiodes having a same surface area as two charge transfer MOS transistors (M4, M5), and as one storage diode (D1), a cathode of each photodiode being connected to a cathode of the storage diode via one of the charge transfer MOS transistors;

a second active area (18) of doped single-crystal silicon arranged next to a portion of the first active area (10) associated with the second photodiode (D3) and corresponding to a

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precharge switch having a first terminal connected to the cathode of the storage diode (D1) and a second terminal connected to a reference voltage (33); and

a third active (20) doped single-crystal silicon area arranged next to the portion of the first active area (10) associated with the first photodiode (D2) and corresponding to two read MOS transistors (M2, M3) in series, the gate (GM2, GM3) of one of the read transistors being connected to the cathode of the storage diode (D1) and the drain (DM2, DM3) or the source (SM2, SM3) of one of the read transistors (M2, M3) being connected to a processing system.

AAPA differs from the claimed invention by not showing the surfaces of the second and third active areas exposed. However, Pellegrini teaches the active area of the photodecting is opened (exposed) (column 4, lines 52-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Pellegrini into the device taught by AAPA in order to release the electrons from the photodiodes.

The combined device differs from the claimed invention by not showing the second and the third active areas are identical. However, Tullis teaches the areas of active areas are identical (column 8, lines 12-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tullis into the device taught by AAPA and Pellegrini in order to get the same gain of electrons in the active areas.

Regarding claim 2, the combined device shows the second (AAPA; 18) and third (AAPA; 20) active areas have substantially identical surface areas.

Regarding claim 3, the combined device shows the first, second, and third active areas (AAPA; 10, 18, 20) are rectangular, the second and third active areas (AAPA; 18, 20) being of

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same dimensions and substantially aligned at a same distance from a side of the first active area (AAPA; 10).

Regarding claim 8, the combined device shows the gates (AAPA; GM4, GM5) of the charge transfer MOS transistors (AAPA; M4, M5) correspond to portions of polysilicon strips (AAPA; 14, 16), which extend between the second and third active areas (AAPA; 18, 20).

Regarding claim 9, AAPA (figures 1-4) teaches a monolithic photodetector comprising:

a first active area (10) of doped single-crystal silicon including first (D2) and second (D3) photodiodes having a same surface area as two charge transfer MOS transistors (M4, M5), and as one storage diode (D1);

a second active area (18) of doped single-crystal silicon arranged next to a portion of the first active area (10) associated with the second photodiode (D3) and including a precharge switch; and

a third active doped (20) single-crystal silicon area arranged next to the portion of the first active area (10) associated with the first photodiode (D2) and including two read MOS transistors (M2, M3) in series.

AAPA differs from the claimed invention by not showing the surfaces of the second and third active areas exposed. However, Pellegrini teaches the active area of the photodecting is opened (exposed) (column 4, lines 52-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Pellegrini into the device taught by AAPA in order to release the electrons from the photodiodes.

The combined device differs from the claimed invention by not showing the second and the third active areas are identical. However, Tullis teaches the areas of active areas are identical

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(column 8, lines 12-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tullis into the device taught by AAPA and Pellegrini in order to get the same gain of electrons in the active areas.

Regarding claim 10, the combined device shows the second (AAPA; 18) and third (AAPA; 20) active areas have substantially identical surface areas.

Regarding claim 11, the combined device shows the first, second, and third active areas (AAPA; 10, 18, 20) are rectangular, the second and third active areas (AAPA; 18, 20) being of same dimensions and substantially aligned at a same distance from a side of the first active area (AAPA; 10).

Regarding claim 16, the combined device shows the gates (AAPA; GM4, GM5) of the charge transfer MOS transistors (AAPA; M4, M5) correspond to portions of polysilicon strips (AAPA; 14, 16), which extend between the second and third active areas (AAPA; 18, 20).

3. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Pellegrini in view of Tullis, and further in view of US Patent No. 6,392,279 to Toyofuku.

Regarding claim 4, the disclosures of AAPA, Pellegrini and Tullis are discussed as applied to claims 1-3 and 8 above.

The combined device differs from the claimed invention by not showing a MOS transistor with two parallel gates. However, Toyofuku (figures 1A-2C) teaches MOS transistor with dual gates (7g). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Toyofuku into the device taught by

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AAPA, Pellegrini and Tullis in order to improve the short-channel effects and provide high current drive between two gates.

Regarding claim 12, the disclosures of AAPA, Pellegrini and Tullis are discussed as applied to claims 9-11 and 16 above.

The combined device differs from the claimed invention by not showing a MOS transistor with two parallel gates. However, Toyofuku (figures 1A-2C) teaches MOS transistor with dual gates (7g). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Toyofuku into the device taught by AAPA, Pellegrini and Tullis in order to improve the short-channel effects and provide high current drive between two gates.

Allowable Subject Matter

Claims 5-7 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
January 26, 2005



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